REMARKS

Applicant has made changes to the specification on page 12, lines 14 and 16. Applicant respectfully submits that these changes nullify any need to make the change requested by the Examiner in the drawings.

Applicant respectfully submits that claims 28 and 60 are proper as presently written. Claim 28 includes the recitation of claim 27. This makes claim 28 different from claim 23, particularly since claim 27 includes the recitation of claim 24. Claim 60 recites that the power applied in the chamber to etch the surface of the wafer is in the order of 600-1200 watts. This is not recited in claim 59 for the step of etching the wafer.

In paragraph 4, entitled "Claim Rejections – 35 U.S.C. 112," the Examiner has provided paragraphs 1-37 to specify changes that applicant should make in the claims. Applicant will use the same paragraph numbers as the Examiner in discussing the changes requested by the Examiner to be made in the claims. Where applicant has made the changes suggested by the Examiner, there is no discussion. In addition to the changes suggested by the Examiner, applicant has made a number of other changes in the claims to correct informalities noted by applicant's attorney upon a further study of the claims. As now written, all of the claims are believed to be definite.

6. Applicant respectfully submits that the word "deposition" in claim 61 and 59 is definite. However, applicant has removed the word "deposition" from claim 59 and has specified in claim 1 that the deposition is of a material.

7. Applicant believes that the phrase "cleaning materials" is definite in claims 1 and 29. Applicant does not believe that he is under any obligation to recite in these claims how the impurities are cleaned from the wafer and what structure in the claims performs the cleaning. This is particularly true since the Examiner has not been able to cite any references against claims 1 and 29. However, applicant has amended the claims to remove any recitation of "cleaning impurities" in claims 1 and 29.

8. In paragraph 8, the Examiner objected to the phrase "creating microscopic roughness" in claims 1, 22, 29 and 39 as being vague and indefinite. According to the Examiner, it is not clear from the claims how the microscopic roughness is created and what structure in the claims performs the roughness process. Applicant believes that the phrase "creating microscopic roughness" is definite and that applicant is under no obligation to recite how the microscopic roughness is created. Furthermore, it is unusual (not the normal practice) to recite <u>structure</u> for performing a step such as the microscopic roughness process.

9. The Examiner has indicated that there is insufficient antecedent basis for "a deposition" in claim 5. Applicant's attorney has been in patent practice for approximately 55 years and has proceeded on the basis that the word "a" preceding a noun overcomes any rejection on the ground that there is no antecedent basis for the noun. If applicant cannot recite a new element in a claim by using the word "a", applicant would be prevented from reciting any element in the claim. However, applicant has added the words "of a material" in claim 1, line 5, to define the deposition.

11. Applicant does not believe that the phrase "removing impurities" in claims 5, 11, 22, 35 and 39 is vague or indefinite. Applicant also does not believe that he is under any obligation to recite in these claims how the impurities are removed from the wafer. Applicant certainly does not believe that he is under any obligation to recite structure in a method claim. However, applicant has removed the phrase "removing impurities" from claims 5, 11, 22, 35 and 39.

12. Claims 5, 11, 48, 50, 52 and 53 have been rejected by the Examiner on the grounds that the phrase "depositing a chromium layer with an intrinsic tensile stress" is vague and indefinite. The rationale by the Examiner for the rejection is that it is not clear what creates the intrinsic tensile stress in the chromium layer. Applicant is not required to recite in the claims technological hypotheses of what causes certain physical phenomena to occur. This is particularly true since the Examiner has not been able to cite any prior art against the claims. However, applicant has amended claims 5, 11, 48, 52 and 53 to recite that the intrinsic tensile stress created by the chromium layer is low.

13. The Examiner has rejected claims 5 and 56 on the grounds that the phrase "depositing a layer of nickel vanadium with an intrinsic stress" is vague and indefinite. According to the Examiner, these claims are vague and indefinite because it is not clear what creates the intrinsic tensile stress in the nickel-vanadium layer. Applicant refers the Examiner to paragraph 12 to explain why applicant disagrees with the position of the Examiner. For example, applicant is not required to recite in the claims technological hypotheses or what causes certain physical phenomena to occur.

16. Claim 6 has been rejected in paragraph 16 on the ground that a "minimal amount" is vague and indefinite. The Examiner has based his rejection on the ground that it is not clear what a minimal amount is. Applicant has amended claim 6 to recite that a low rate of flow of an inert gas is provided on the wafer layer when the chromium layer is deposited on the surface of the wafer, thereby to minimize the presence of the inert gas in the chromium layer.

22. Claim 15 has been rejected on the basis that there is insufficient antecedent basis for "a waferland" in claim 15. As previously indicated, the use of the word "a" preceding a noun provides an antecedent basis for the noun.

23. The Examiner has rejected claims 15 and 34 on the basis that there is insufficient antecedent basis for "a layer of chromium" in these claims. As applicant has previously indicated, the recitation of an element preceded by the word "a" provides an antecedent basis for the element.

27. Applicant respectfully submits that the recitation of "the metal layer" in claim 18, line 5 has an antecedent basis. Applicant respectfully refers the Examiner to the recitation of "a layer of metal" in claim 18, line 3.

29. According to the Examiner, the language "the deposition" in claims 21 and 26 has an insufficient antecedent basis. Claim 21 is dependent from claim 18 through claim 20. The words "the deposition in claim 21, line 4, have an antecedent basis in claim 18, line 6. Claim 26 is dependent from claim 22 through claim 24. The words "the deposition" in claim 26, line 5, have an antecedent basis in claim 22, line 7.

30. The Examiner has rejected claims 23 and 27 on the basis that the words "the sub-assembly" do not have an antecedent basis in the claims. Applicant has amended claim 23 to make it dependent from claim 22. Applicant has also amended "the component or sub-assembly" in claim 23, line 4, to "a component or sub-assembly". Applicant does not see the words "component" or "sub-assembly" in claim 27.

32. The Examiner has rejected claims 44, 48, 51 and 53 because the phrase "In combination" is vague and indefinite. Applicant has been using the preamble "In combination" in claims for more than 50 years. In that period of time, no Examiner has rejected applicant's claims because of the use of this preamble. However, applicant has adjusted this preamble to read "In combination for performing electrical functions." If this is not acceptable to the Examiner, applicant will be willing to change the word "combination" to - -apparatus- -.

The Examiner has also rejected claims 44, 48, 51 and 53 on the ground that it is not clear what type of semiconductor device applicant is making claim for. Applicant is not attempting to claim any type of semiconductor device. Applicant is attempting to claim a method and apparatus for preparing a surface of a wafer so that applicant can fixedly attach a component or sub-assembly to a wafer.

34. The Examiner has considered the phrase "depositing a layer of nickel vanadium with an intrinsic compressive stress" in claims 48 and 53 to be vague and indefinite because it is not clear what creates the intrinsic compressive stress in the chromium layer. As applicant has indicated in paragraph 12, applicant is under no obligation to recite in the claims technological hypotheses of what causes certain physical

phenomena to occur. However, applicant has amended claims 48 and 53 to recite that the intrinsic compressive stress in the nickel vanadium layer is low.

37. The words "the metal layer" in claim 57, lines 4 and 5 have an antecedent basis in claim 57, line 2. Furthermore, applicant has amended claim 57 to recite that the metal layer recited in claim 57, lines 4 and 5 is selected from the group consisting of copper, gold and silver. There is antecedent basis for this recitation.

Applicant has added claims 65-69 in this amendment. Applicant respectfully submits that claims 1-69 as now written are definite.

Applicant appreciates the indication by the Examiner that the claims distinguish over the references cited by the Examiner.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

In light of the above amendments and remarks, applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Page 3, line 14:

In a preferred embodiment of the invention, a plurality of successive layers are firmly adhered to one another and to a wafer surface and an electrical component or sub-assembly even when the wafer surface is not even and the layers are bent. The wafer surface is initially cleaned by an ion bombardment of an inert gas (e.g. argon) on the wafer surface in an RF discharge at a relatively high gas pressure. The wafer surface is then provided with a microscopic roughness by applying a low power [and] so that the inert gas (e.g. argon) ions do not have sufficient energy to etch the surface.

Pages 12-13, line 14

Pages 12-13, line 16:

Figure 5 is a curve [32] <u>36</u> showing the relationship between RF bias power in watts along the horizontal axis and stress in E9 dynes per square centimeter along the vertical axis when the nickel vanadium layer 20 is deposited on the chromium layer 18. The curve [32] <u>36</u> shown in Figure 5 is provided for deposition equipment such as the equipment shown in Figure 4. Figure 5 shows how the stress in the nickel-vanadium layer 20 decreases with increases in the RF power applied.

IN THE CLAIMS

1. (Amended) In a method of etching a surface of a wafer with a microscopic roughness to prepare the wafer surface for receiving a deposition of a material on the wafer surface, [including] the steps of

[cleaning impurities] removing a thin layer from the surface of the wafer to eliminate any impurities from the surface of the wafer, and

thereafter creating [a] the microscopic roughness on the surface of the wafer to receive a deposition of the material on the surface.

2. (Amended) In a method as set forth in claim 1 wherein

the microscopic roughness on the [cleaned] surface of the wafer is created by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

4. (Amended) In a method as set forth in [claims] claim 1 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on the surface of the wafer.

5. (Amended) In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing [impurities] a thin layer from the surface of the wafer,

thereafter depositing a chromium layer with [an] a low intrinsic tensile stress on the cleaned surface of the wafer, and

thereafter depositing a layer of nickel vanadium with an intrinsic stress on the surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer.

6. (Amended) In a method as set forth in claim 4 wherein

a microscopic roughness is produced on the surface of the wafer after the [surface] thin layer of the wafer has been [cleaned] removed from the surface of the wafer and wherein

the chromium layer is thereafter deposited on the microscopically rough surface of the wafer and wherein

a [minimal amount] low rate of flow of an inert gas is [produced] provided on the wafer layer when the chromium layer is deposited on the surface of the wafer thereby to minimize the presence of the inert gas in the chromium layer.

7. (Amended) In a method as set forth in claim [4] 5 wherein

a waferland is disposed in an abutting relationship with the wafer and wherein

a layer of chromium is deposited on the surface of the waferland before etching the surface of the wafer.

9. (Amended) In a method as set forth in claim [4] 5 wherein

the chromium is deposited in a layer on the microscopically rough surface of the wafer to produce an intrinsic tensile stress with a low stress value in the chromium layer and wherein

the nickel vanadium layer is deposited on the surface of the chromium layer to produce [an] <u>a low</u> intrinsic compressive stress with a value to neutralize the <u>low</u> intrinsic tensile stress in the chromium layer.

11. (Amended) In a method of providing for an attachment of an electrical component to a wafer, [including] the steps of:

removing [impurities] <u>a thin layer</u> from the surface of the wafer, and

depositing a chromium layer [in an] <u>with a low</u> intrinsic tensile stress on the surface of the wafer [with a low stress value] after the removal of the [impurities] <u>thin layer</u> from the surface of the wafer.

12. (Amended) In a method as set forth in claim [10] <u>11</u> wherein

the surface of the wafer is provided with a microscopic roughness after the [impurities have] <u>thin layer has</u> been removed from the surface of the wafer and wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value.

13. (Amended) In a method as set forth in claim [10] <u>11</u> wherein

the chromium layer is deposited on the surface of the wafer in a magnetron with [substantially] no RF bias in the magnetron and with a low flow rate of molecules of an inert gas in the magnetron.

14. (Amended) In a method as set forth in claim [12] <u>11</u> wherein

[the inert gas is argon and the flow rate of the] <u>a chamber is provided in which to perform the recited steps and wherein</u> molecules of [the] <u>an</u> inert gas [in] <u>flow through</u> the chamber [is] in [the] <u>an</u> order of three (3) to five (5) standard cubic centimeters [(5 sccm)] per minute (3-5 sccm).

15. (Amended) In a method as set forth in claim 12 wherein

a chamber is provided in which to perform the recited steps and wherein

a waferland is disposed in the chamber to support the wafer and wherein a layer of chromium is deposited on the waferland before [etching the wafer surface] the chromium layer is deposited on the surface of the wafer.

16. (Amended) In a method as set forth in claim 11 wherein

a waferland and a chamber are provided and the wafer and the waferland are disposed in the chamber and wherein

the chromium layer is deposited on the surface of the wafer in [a] the chamber with [substantially] no RF bias on the waferland in the chamber and with a low flow rate of molecules of an inert gas in the chamber,

the inert gas is argon and the flow rate of the molecules of the inert gas in the chamber is in the order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm)[, and

a waferland is disposed in the chamber to support the wafer and wherein a layer of chromium is deposited on the waferland before etching the wafer surface].

17. (Amended) In a method of providing for an attachment of an electrical component or sub-assembly to a wafer, the steps of:

removing [impurities] a thin layer from the surface of the wafer,

depositing a layer of chromium on the surface of the wafer with [an] a low intrinsic tensile stress, and

depositing a nickel vanadium layer on the surface of the chromium layer with an RF bias power to produce [an] a low intrinsic compressive stress in the nickel vanadium layer for neutralizing the low intrinsic tensile stress in the chromium layer.

18. (Amended) In a method as set forth in claim [16] 17 wherein

a layer of metal selected from the group consisting of gold, silver and copper is deposited on the surface of the layer of nickel vanadium and wherein

the nickel vanadium layer has [an] a low intrinsic compressive stress to neutralize the low intrinsic tensile stress in the chromium layer and any stress in the metal layer selected from the group consisting of gold, silver and copper.

20. (Amended) In a method as set forth in claim 18 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland before [etching the wafer surface] the thin layer is removed from the surface of the wafer and wherein

the electrical component is soldered to the layer of the metal selected from the group consisting of gold, silver and copper.

21. (Amended) In a method as set forth in claim 20 wherein

a lens shield is disposed in a spaced relationship to the waferland and the lens shield is grounded and wherein

the RF bias power for the deposition of the layer of nickel vanadium is provided between the waferland and the grounded lens shield.

22. (Amended) In a method of providing for an attachment of an electrical component to a wafer, [including] the steps of:

[removing impurities] <u>removing a thin layer</u> from the surface of the wafer,

<u>thereafter</u> providing the surface of the wafer with a microscopic roughness,

<u>thereafter</u> depositing a layer of chromium on the microscopically rough surface of the wafer with a low intrinsic tensile stress, and

<u>thereafter</u> depositing a layer of nickel vanadium on the surface of the wafer with a low intrinsic compressive stress.

23. (Amended) In a method as set forth in claim 21 wherein

a layer of a metal selected from a group consisting of gold, nickel and copper is deposited on the surface of the nickel vanadium layer and wherein

[the] <u>a</u> component or sub-assembly is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

28. (Amended) In a method as set forth in claim 27 wherein

a layer of a metal selected from a group consisting of gold, nickel and copper is deposited on the surface of the nickel vanadium layer and wherein

the component or sub-assembly is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

29. (Amended) In a method of providing a deposition on a surface of a wafer, the steps of:

[cleaning impurities] <u>removing a thin layer</u> from the surface of the wafer <u>to eliminate impurities from the surface of the wafer</u>,

creating a microscopic roughness on the surface of the wafer, and

depositing a chromium layer with [an] a low intrinsic tensile stress on the microscopically rough surface of the wafer [by providing the layer with no RF bias].

32. (Amended) In a method as set forth in claim [29] 30 wherein

the microscopic roughness is produced on the surface of the wafer by providing the molecules of the inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

33. (Amended) In a method as set forth in claim [32] 29 wherein

no RF bias is provided when the chromium layer is deposited on the surface of the wafer and wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and wherein

an inert gas having a low flow rate is passed through the chamber, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent the inert gas from being entrapped in the chromium layer and wherein

the inert gas is argon.

35. (Amended) In a method of preparing a wafer surface for receiving an electronic component, the steps of:

removing [impurities] a thin layer from the surface of the wafer,

thereafter creating a microscopic roughness on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer, and

thereafter depositing a chromium layer on the microscopically rough surface of the wafer in a chamber in which a minimal amount of an inert gas is passed through the chamber during the deposition to prevent molecules of the inert gas from being entrapped in the chromium layer.

37. (Amended) In a method as set forth in claim 35 wherein

the chromium layer is deposited on the surface of the wafer under tension with a [minimal] low amount of stress.

38. (Amended) In a method as set forth in claim 36 wherein

the chromium layer is deposited on the surface of the wafer with a [minimal] low amount of intrinsic tensile stress.

39. (Amended) In a method of providing a deposition on a surface of a wafer [surface] for receiving an electronic component on the wafer surface, the steps of:

removing [impurities] a thin layer from the surface of the wafer,

creating a microscopic roughness on the surface of the wafer, and

atomically bonding a chromium layer to the microscopically rough surface on the wafer.

41. (Amended) In a method as set forth in claim 39, the step of:

providing a [minimal amount of] low intrinsic tensile stress in the chromium layer.

44. (Amended) In combination for performing electrical functions,

a wafer having a clean surface with a microscopic roughness, and

a layer of chromium deposited on the microscopically rough surface of the wafer with a [minimal amount of] low intrinsic tensile stress in the chromium layer.

45. (Amended) In a combination as set forth in claim 44 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer with a [minimal amount of] low intrinsic tensile stress.

48. (Amended) In combination for performing electrical functions,

a wafer,

a chromium layer deposited on the wafer with [an] a low intrinsic tensile stress, and

a layer of nickel vanadium deposited on the chromium layer in firmly adhered relationship to the chromium layer with [an] a low intrinsic compressive stress.

49. (Amended) In a combination as set forth in claim 48,

the chromium layer being under [an] the low intrinsic tensile stress [with a minimal value] and the nickel vanadium layer being under [an] the low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer.

50. (Amended) In a combination as set forth in claim 48,

the chromium in the chromium layer having [an] the low intrinsic tensile stress for bonding to the microscopically rough wafer surface,

the chromium in the chromium layer having an atomic bonding with the microscopically rough surface on the wafer.

51. (Amended) In combination for performing electrical functions,

a wafer having a clean surface with a microscopic roughness, and

a chromium layer deposited on the microscopically rough surface of the wafer and atomically bonded to the microscopically rough wafer surface.

52. (Amended) In a combination as set forth in claim 51,

the chromium layer having [an] <u>a low</u> intrinsic tensile stress for bonding to the microscopically rough wafer surface.

53. (Amended) In combination <u>for performing electrical functions</u>,

a wafer having a clean surface,

a chromium layer disposed on the clean surface of the wafer with an intrinsic tensile stress, and

a nickel vanadium <u>layer</u> deposited on the chromium layer with [an] <u>a low</u> intrinsic compressive stress.

54. (Amended) In a combination as set forth in claim 53 wherein

the <u>low</u> intrinsic compressive stress of the nickel vanadium layer substantially neutralizes the <u>low</u> intrinsic tensile stress of the chromium layer.

56. (Amended) In a combination as set forth in claim 52,

a layer of a metal selected from the group consisting of copper, gold and silver and disposed on the nickel vanadium layer with [an] <u>a low</u> intrinsic tensile stress.

57. (Amended) In a combination as set forth in claim 53 wherein

a layer of a metal selected from the group consisting of copper, gold and silver is [disposed] <u>deposited</u> on the nickel vanadium layer and wherein

the nickel vanadium layer substantially neutralizes any intrinsic stress in the metal layer <u>selected from the group consisting of copper, gold and silver</u>.

59. (Amended) In a method of etching a surface of a wafer with a microscopic roughness [to prepare the wafer surface for receiving a deposition], the steps of:

providing a flow of an inert gas in the order of forty (40) to fifty (50) standard cubic centimeters per minute through a chamber containing the wafer to etch a microscopic layer of material with impurities from the surface of the wafer and provide an atomic roughness to the wafer surface,

thereafter providing a flow of an inert gas through the chamber at a flow rate of approximately forty (40) to fifty (50) standard cubic centimeters per minute and a power in the order of six hundred watts (600 W) to twelve hundred watts (1200 W) to clean the surface of the wafer and increase the roughness of the wafer surface,

disposing the wafer on a waferland, and

then providing a flow of an inert gas at a rate through the chamber at a low power in the order of fifty watts (50 W) to one hundred watts (100 W) [between the waferland and ground] to provide the surface of the wafer with [a] the microscopic roughness.

65. (New) In a method as set forth in claim 29 wherein

the chromium layer is deposited with a low intrinsic tensile stress on the microscopically rough surface by providing the layer with no RF bias.

66. (New) In a method as set forth in claim 29 wherein

the microscopic roughness is created on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

67. (New) In a method as set forth in claim 2 wherein

the inert gas is argon and wherein

the wafer disposed on a waferland and wherein

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on a the surface of the wafer.

68. (New) In a method as set forth in claim 22 wherein

the microscopic roughness on the surface of the layer is created by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a coefficient energy to create the microscopic roughness on the surface of the wafer.

69. (New) In a method as set forth in claim 39 wherein

the microscopic roughness is created on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but a sufficient energy to create the microscopic roughness on the surface of the wafer.